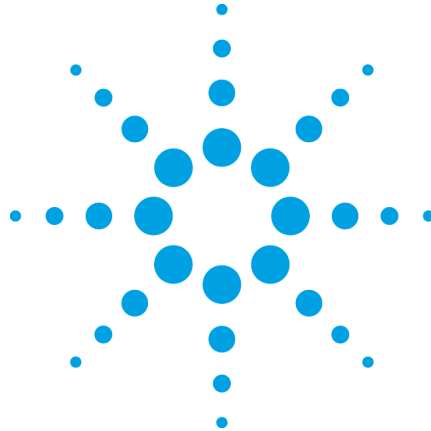


10 Gigabit Ethernet and the XAUI interface

Product Note



New testing challenges for the

71612C

12.5 Gb/s error performance analyzer



Agilent Technologies

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Introduction

The 10 Gigabit Ethernet Standard

In common with earlier IEEE 802.3 standards, 10 Gigabit Ethernet will ultimately define a standard which ensures interoperability between products from different vendors. The standard primarily specifies the physical layers and only a small change will be made to the media access control (MAC). The adoption of cost effective, robust technologies largely enabled Ethernet to dominate the LAN market; the same approach is being used in the development of the 10 Gigabit Ethernet (10GbE). A significant difference however is that 10GbE represents the merging of data communications and telecommunications.

In the International Standards Organization's Open Systems Interconnection (OSI) model, Ethernet is fundamentally a Layer 2 protocol. 10 Gigabit Ethernet uses the IEEE 802.3 Ethernet Media Access Control (MAC) protocol, the IEEE 802.3 Ethernet frame format, and the minimum and maximum IEEE 802.3 frame size.

Just as Gigabit Ethernet remained true to the Ethernet model, 10 Gigabit Ethernet continues the natural evolution of Ethernet in speed and distance. Since it is a full-duplex only and fiber-only technology, it does not need the carrier-sensing, multiple-access with collision detection, (CSMA/CD) protocol that defines slower, half-duplex Ethernet technologies. In every other respect, 10 Gigabit Ethernet remains true to the original Ethernet model.

An Ethernet PHYsical layer device (PHY), which corresponds to Layer 1 of the OSI model, connects the media to the MAC layer, which corresponds to OSI Layer 2. Ethernet architecture further divides the PHY (Layer 1) into a Physical Media Dependent (PMD) and a Physical Coding Sublayer (PCS). Optical transceivers, for example, are PMDs. The PCS is made up of coding (e.g., 64/66b) and a serialiser or multiplexing functions.

Port types

The recently ratified 802.3ae standard (IEEE Draft P802.3ae/D5.0, May 1, 2002) defines two PHY types: the LAN PHY and the WAN PHY. The WAN PHY has an extended feature set added onto the functions of a LAN PHY.

The 802.3ae standard supports several physical layers signaling systems or port types for use with both multi-mode and single-mode plant and distances up to 40 km. The implementation notation is "10GBASE-(X)(Y)" where:

X is S, L, or E

S is the short wavelength 850 nm system
L is the 1300 nm long wavelength system
E is the 1550 nm extended wavelength system

Y is R, W, or X

X uses 8B/10B coding (25% overhead)
R uses 64B/66B coding (about 3% overhead)
W uses an STS-192 encapsulation of the 64B/66B encoded data for use with a SONET payload

Six of the port types use bit serial optical transmission whilst the seventh multiplexes MAC data across four wavelengths. The WWDM physical layer can support both multi-mode and single mode .

Table 1 lists the two categories of port types:

- LAN PHY for native Ethernet applications
- WAN PHY for connection to 10 Gb/s SONET/SDH

Layered architecture

Figure 1 depicts the layered model for 10 Gbit Ethernet and the sub-layers for the two categories of PHY (LAN and WAN).

10 Gigabit Ethernet MAC

The standard MAC data rate for 10 Gigabit Ethernet is 10 Gb/s; this is the rate at which the MAC transfers information to the PHY. For WAN PHY operation the MAC data rate is reduced to the slightly lower data rate of SONET/SDH equipment by dynamically adapting the interframe spacing.

WWDM LAN PHY

This uses a physical coding sublayer (PCS) based on four channels or lanes of 8B/10B coded data. Each lane operates at 2.5 Gb/s with a coded line rate of 3.125 Gb/s.

Serial LAN PHY

Initially it appeared attractive to reuse the 8B/10B code used with Gigabit Ethernet, however it was soon realised that the resulting 12.5 Gbaud would require costly technical issues to be solved and raise the development cost of effective serial implementation. It was therefore decided to employ a more efficient 64B/66B code, which reduced the serial baud rate to 10.3125 GBaud. Table 1 also shows the three wavelengths employed and the maximum link lengths.

Serial WAN PHY

For this PHY an additional sub-layer known as the WAN Interface Sub-layer (WIS) is required between the PCS and the serial PMA. The position of this in the 10GBASE-W architecture is shown in Figure 1. The WIS maps the output of the serial PCS into a frame, based on SONET/SDH practice and vice versa, and processes the frame overhead including pointers and parity checks. The line rate is 9.95328 Gb/s.

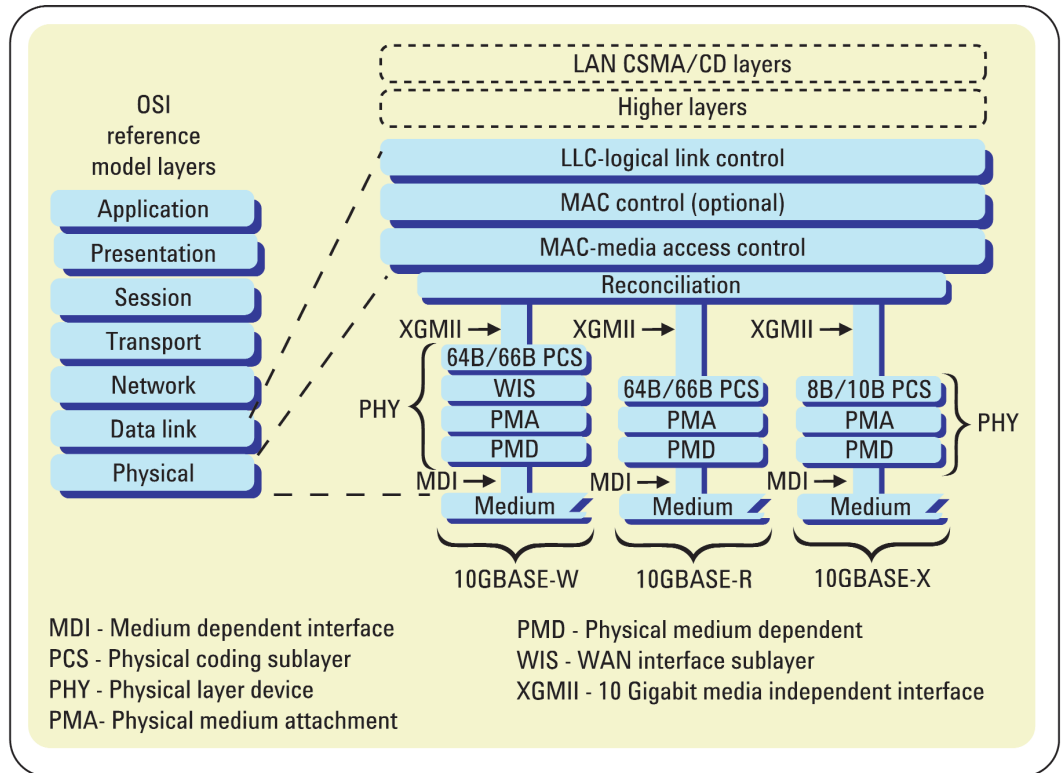


Figure 1. Architectural Positioning of 10 Gigabit Ethernet

Table 1. 10 Gigabit Ethernet Port Types

Description	Name	Comments
850 nm serial LAN PHY	10 GBASE-SR	Directly modulated VCSEL, MMF, 2–300 m
1310 nm serial LAN PHY	10 GBASE-LR	Directly modulated DFB laser, SMF, 2–10 km
1550 nm serial LAN PHY	10 GBASE-ER	Modulator, DFB laser, SMF, 2–40 km
1310 nm WWDM LAN PHY	10 GBASE-LX4	Directly modulated VCSEL or DFB, MMF (300 m) or SMF (2–10 km)
850 nm serial WAN PHY	10 GBASE-SW	Directly modulated VCSEL, MMF, 2–300 m
1310 nm serial WAN PHY	10 GBASE-LW	Directly modulated DFB laser, SMF, 2–10 km
1550 nm serial WAN PHY	10 GBASE-EW	Modulator, DFB laser, SMF, 2–40 km

Chip Interface (XAUI)

This description of XAUI is freely adapted from a white paper published by the 10 Gigabit Ethernet Alliance. Among the many technical innovations of the 10 Gigabit Ethernet Task Force is an interface called the XAUI (pronounced “Zowie”). The ‘AUI’ portion is borrowed from the Ethernet Attachment Unit Interface. The “X” represents the Roman numeral for ten and implies ten Gigabits. The XAUI is designed as an interface extender, and the interface, which it extends, is the XGMII, the 10 Gigabit Media Independent Interface. The XGMII is a 74 signal wide interface (32-bit data paths for each of transmit and receive) that may be used to attach the Ethernet MAC to its PHY. The XAUI may be used in place of, or to extend, the XGMII in chip-to-chip applications typical of most Ethernet MAC to PHY interconnects (See Figure 2).

The XAUI is a low pin count, self-clocked serial bus directly evolved from Gigabit Ethernet. The XAUI interface speed is 2.5 times that used in Gigabit Ethernet. By arranging four serial lanes, the 4-bit XAUI interface supports the ten-times data throughput required by 10 Gigabit Ethernet.

The XAUI employs the same robust 8B/10B transmission code of Gigabit Ethernet to provide a high level of signal integrity through the copper media typical of chip-to-chip printed circuit board traces. Additional benefits of XAUI technology include its inherently low EMI (Electro-Magnetic Interference) due to its self-clocked nature, compensation for multi-bit bus skew—allowing

significantly longer-distance chip-to-chip—error detection and fault isolation capabilities, low power consumption, and the ability to integrate the XAUI input/output within commonly available CMOS processes.

Many component vendors are delivering or have announced XAUI interface availability on standalone chips, custom ASICs (application-specific integrated circuits), and even FPGAs (field-programmable gate arrays). The 10 Gigabit Ethernet XAUI technology is identical or equivalent to the technology employed in other key industry standards such as InfiniBand(TM), 10 Gigabit Fiber Channel, and general purpose copper and optical backplane interconnects. This assures the lowest possible cost for 10 Gb/s interconnects through healthy free market competition.

Specifically targeted XAUI applications include MAC to Physical layer chip and direct MAC-to-optical transceiver module interconnects. The XAUI is the interface for the proposed Ten Gigabit Pluggable optical module definition called the XGP. Integrated XAUI solutions together with the XGP will enable efficient low-cost 10 Gigabit Ethernet direct multi-port MAC to optical module interconnects with only PC board traces in between.

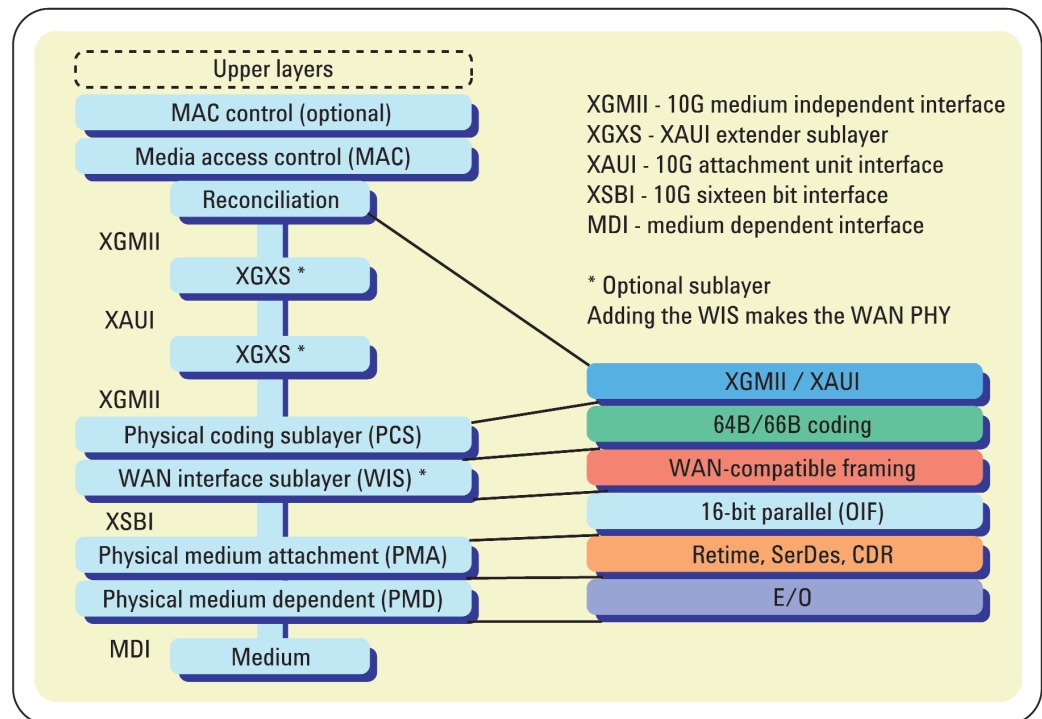


Figure 2. XAUI functions as an extender interface between the MAC and PCS

Summary of XAUI

Figure 3 shows the building blocks of a 10 Gigabit Ethernet transceiver and Figure 4 shows the advantages of selecting XAUI as the interface between the system electronics and the optical transceiver. XAUI eliminates the alternative 36+36 bit wide Tx and Rx PCB trace with its associated skew problems; XAUI mitigates skew in the logic layer. XAUI has its own set of test and measurement opportunities.

Ethernet and Gigabit Ethernet equipment routinely uses front panel connectorised electrically hot-pluggable optical transceivers (Figure 5). The wish was to also use this methodology for

10 Gigabit Ethernet; the XAUI interface provides a narrow electrical interface for such optical transceivers. A Multi-source agreement (MSA) called XENPAK for XAUI-based transceivers has been published. Figure 6 shows the benefits of this methodology.

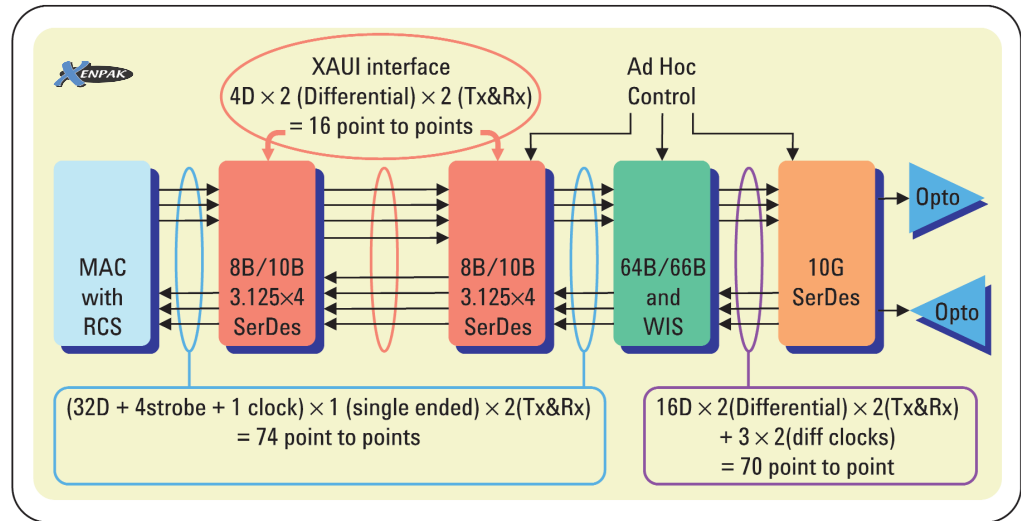


Figure 3. 10 Gig Building Blocks

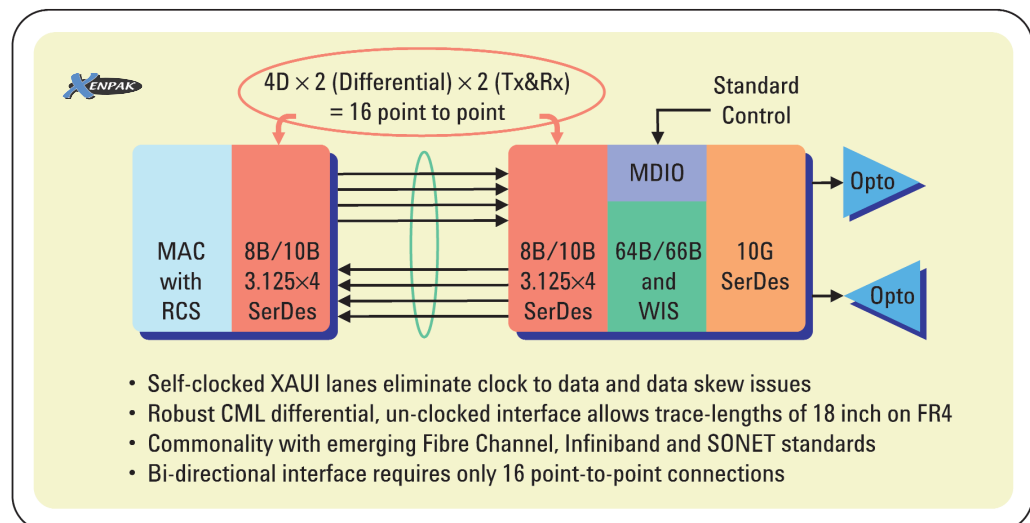


Figure 4. Benefits of Selecting XAUI as interface between system electronics and optical transceiver

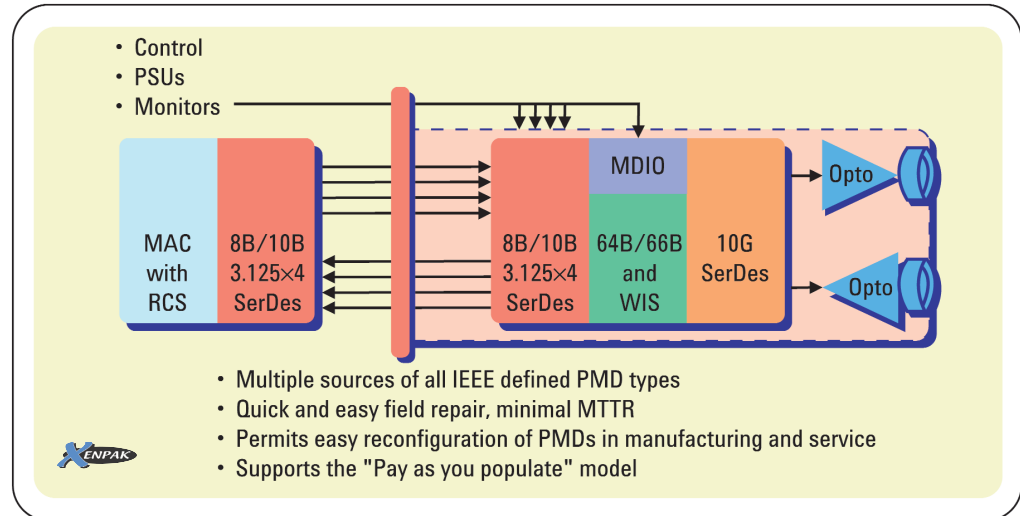


Figure 5. Benefits of front panel hot pluggable transceivers

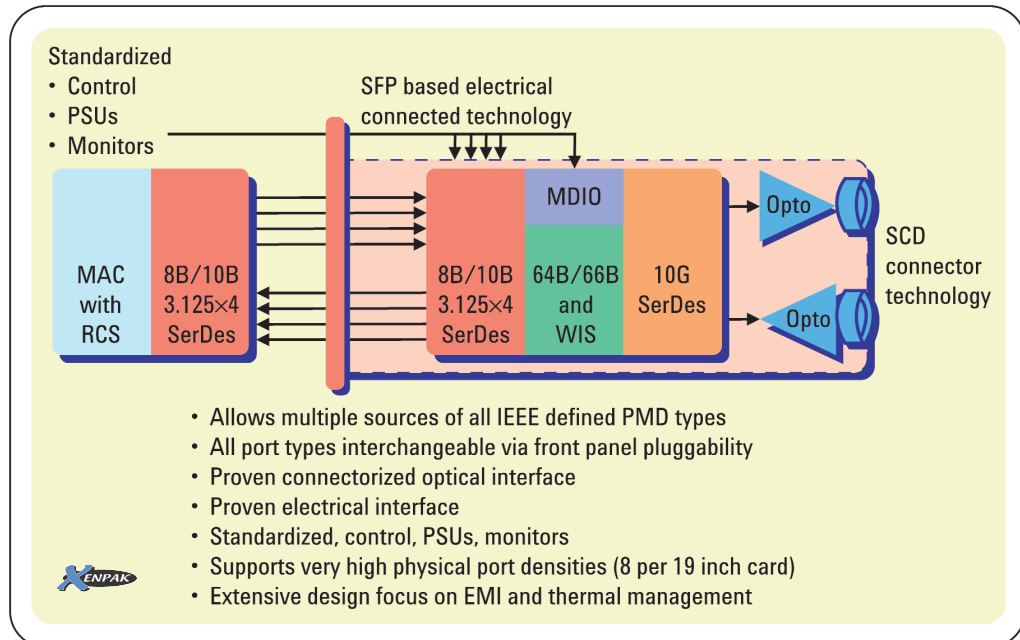


Figure 6. Benefits of Xenpak MSA

Test and measurement opportunities

Test and measurement opportunities for the 71612C 12.5 Gb/s error performance analyzer

A wide range of optical measurements is described in the 802.3ae Standard, including optical transmitter and receiver testing, electrical XAUI test and jitter testing. Many of the tests are essentially eye mask/template measurements. This paper will focus on the tests that specifically require a bit-error-ratio test set (BERT) or error performance analyzer, and will show how the 71612C may be used in these applications.

Figure 7 shows a much simplified block diagram of the elements of a typical Xena 10 Gigabit Ethernet transceiver module, including the coding and scrambling functions. BER testing may be performed at either the XAUI electrical I/O or the 10.3125 Gb/s optical I/O. The internal elastic buffers in the transceiver module or ASIC are effectively disabled by driving the device under test (DUT) with synchronous signals at 3.125 Gb/s and 10.3125 Gb/s. The presence of the scrambler and de-scrambler makes it very difficult to define a test pattern which could be used to test BER from the XAUI interface (4×3.125 Gb/s) to the 10.3125 Gb/s optical output. Although disabling the scrambler of the DUT via its MDIO management interface would seem to offer a work around, in fact this results in unscrambled idle patterns (see below) with inadequate timing information being supplied to the internal clock and data recovery circuit of the DUT. The testing philosophy described in this document therefore assumes that testing of Xena devices is carried out electrically at the 3.125 Gb/s XAUI input and output ports, and separately at the 10.3125 Gb/s optical input and outputs.

The test configurations to be discussed can be divided into two different categories:

- Using the Xena reference clock input port (156.25 MHz) - This port will not be available on the standardised MSA Xena connector, however in the R&D or pilot production phase of development it may be accessible and can be used.
- Using external clock recovery and clock multiplier functions to clock the BERT synchronously with the ref VCO in the Xena device under test.

The XAUI interface is intended for interconnection between ICs; it is a low swing AC coupled differential interface. The AC coupling allows for interoperability between components operating from different supply voltages. The XAUI signal paths are point-to-point connections; each path corresponds to a XAUI lane and comprises two complementary signals making a balanced differential pair. There are four differential paths in each direction – or sixteen connections. These paths are intended to operate up to approximately 50 cm over controlled impedance traces on standard FR4 printed circuit boards.

The XAUI inputs of the device under test may be driven single-ended, for example by the Agilent Technologies 71612C pattern generator sub-rate outputs, however some measurements, such as jitter tolerance may benefit by using baluns on each input when driven from a single-ended source.

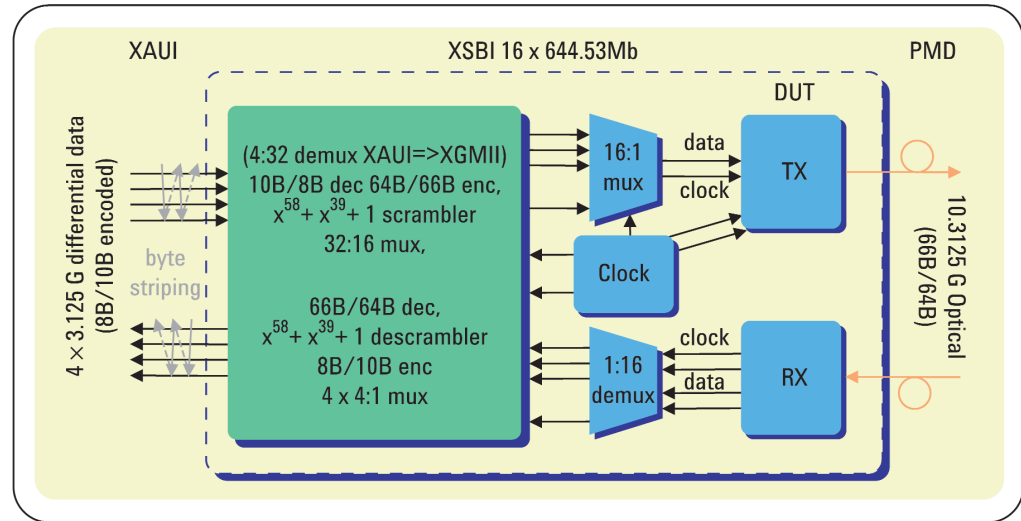


Figure 7. Xenpak module (DUT) simplified block diagram

The Standard specifies that the XAUI receiver shall operate with a BER of less than 10^{-12} in the presence of a reference input signal, which is defined in the Standard by a driver template. This signal is a compliant XAUI transmit signal (differential amplitude as large as 2500 mVp-p and as small as 200 mVp-p).

BER measurement at XAUI I/O (4 x 3.125 Gb/s) using Xenpak reference clock input

To measure BER at the DUT XAUI interface requires four 3.125 Gb/s signals carrying the required test patterns. Four suitable output signals may be generated using the sub-rate outputs of the 71612C BERT; these outputs are at one quarter of the rate of the 71612C main serial output. Therefore to produce four outputs at 3.125 Gb/s, the 71612C clock source must be set up for 12.5 Gb/s operation. Figure 8 shows the diagram of the test set-up to test the XAUI interface with the 71612C using the reference clock input. For reasons, which will become apparent, the most cost-effective solution employs the separate pattern generator and error detector options of the 71612C. The stand-alone error detector option of the 71612C is option UHH. However note that one display can control both pattern generator and error detector – therefore to save cost the error detector may be obtained without a display as Agilent 70843C option UHH.

It is assumed that the DUT is a Xenpak transceiver or ASIC with 10 Gb/s optical I/O as well as the XAUI I/O, however note that a range of ASICs are available with XAUI interfaces – these may also be tested with this basic set-up.

The 156.25 MHz reference clock is best obtained by dividing the 2.5 GHz output of a low phase noise synthesizer by 16; this produces lower clock jitter than would be obtained from a direct 156.25 MHz synthesizer output.

The four XAUI inputs are known as lane 0, lane 1, lane 2 and lane 3. For convenience the sub-rate outputs of the 71612C are labeled similarly. The 71612C sub-rate clock output is used as the clock input for the error detector which is used to measure the BER of each of the four XAUI output lanes one at a time. The BERT clock source and the RF source providing the reference clock for the DUT are synchronised via their 10 MHz reference clocks. The 10.3125 Gb/s optical output is looped back to the 10.3125 Gb/s optical input.

A range of test patterns for XAUI test is defined in Standard 802.3ae (Annex 48A). Many of these are available on the 71612C web page as downloads (see <http://www.agilent.com/cm/rdmfg/hsber/>). The creation of test patterns for XAUI testing requires a detailed knowledge of standard code groups and running disparity rules. A discussion of these is not appropriate in this paper, however Figure 10 lists the basic code groups. These are defined in 8B/10B coded binary form in ANSI X3.230- 1996 'Fibre Channel – Physical and Signaling Interface (FC-PH)(Section 11).

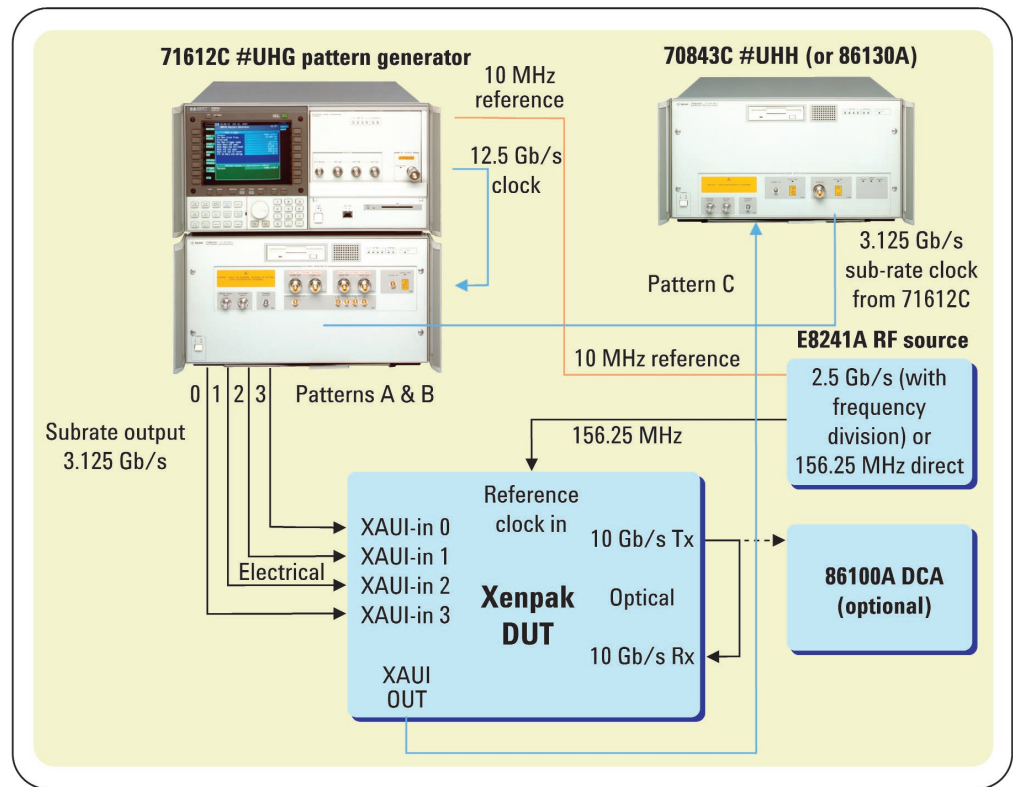


Figure 8. 10 GbE device testing at 3.125 Gb/s – synchronous operation using Xenpak clock input

BER measurements at XAUI I/O (4 x 3.125 Gb/s) using external clock recovery function to synchronize 71612C to Xepak

Following standardization of the Xepak MSA the reference clock input of the Xepak device under test will not be available on the Xepak connector. Figure 9 shows a configuration that may be used for synchronous testing of a Xepak device. In this case 3.125 Gb/s data and clock is recovered from the XAUI output. The data signal is supplied to the error detector, and the clock signal to a four-times clock multiplier. The 12.5 Gb/s output of the multiplier is used as the clock input signal for the pattern generator. Evaluation boards and integrated circuits for those external functions are starting to appear on the market. Note that this particular configuration does not require the 71612C standard clock source to be used.

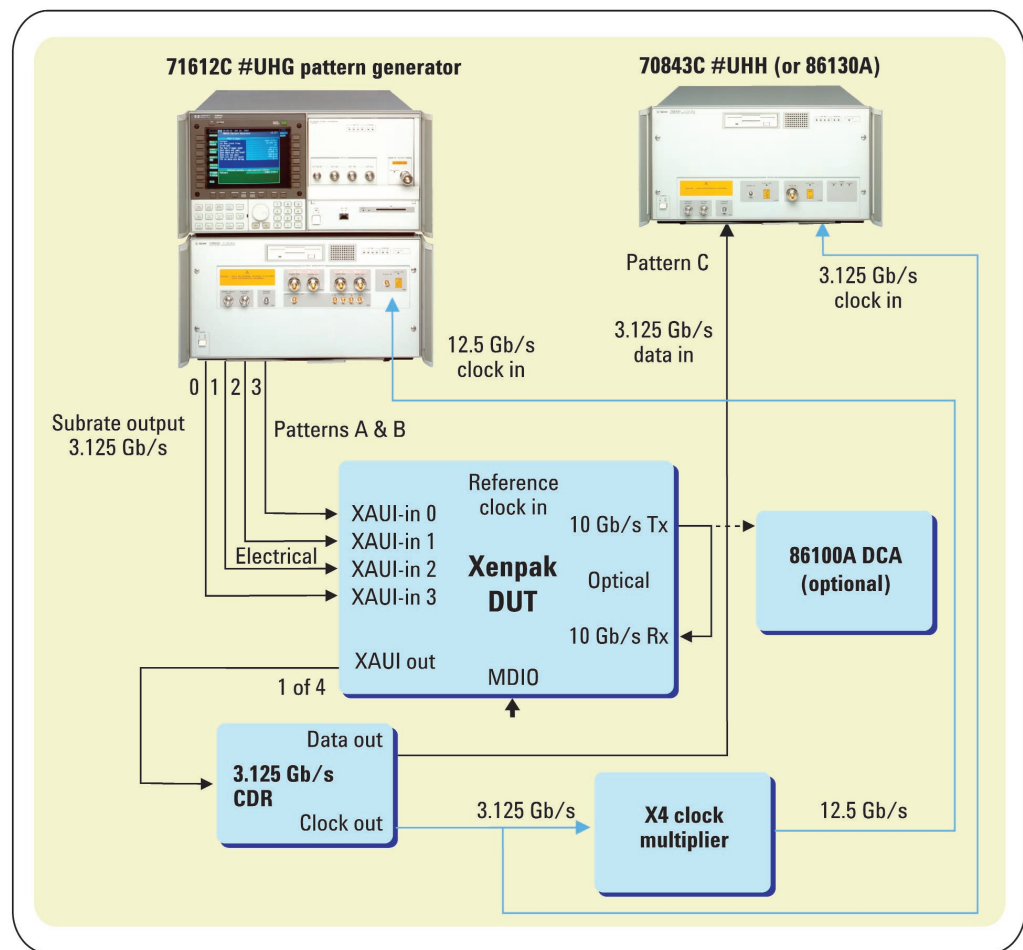
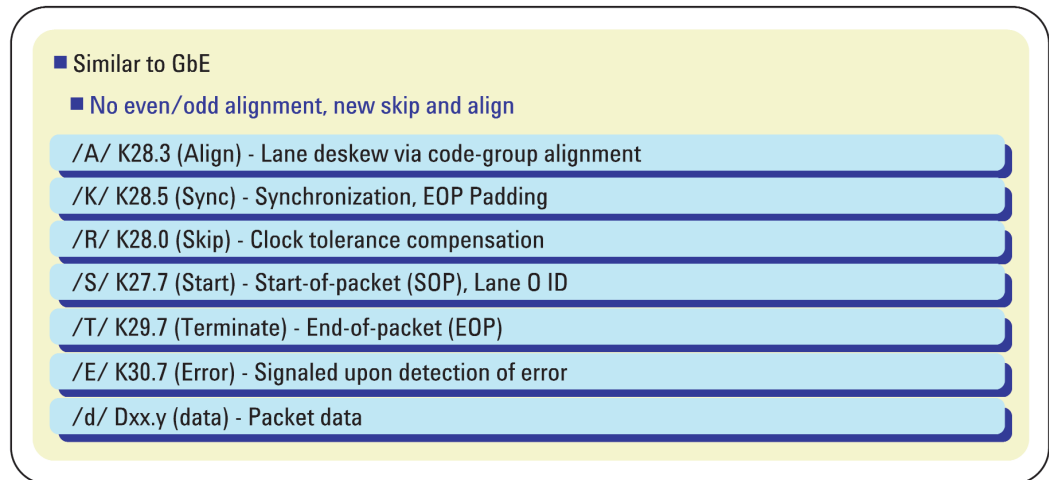


Figure 9. 10 GbE device testing at 3.125 Gb/s - Xepak internal clock used as reference

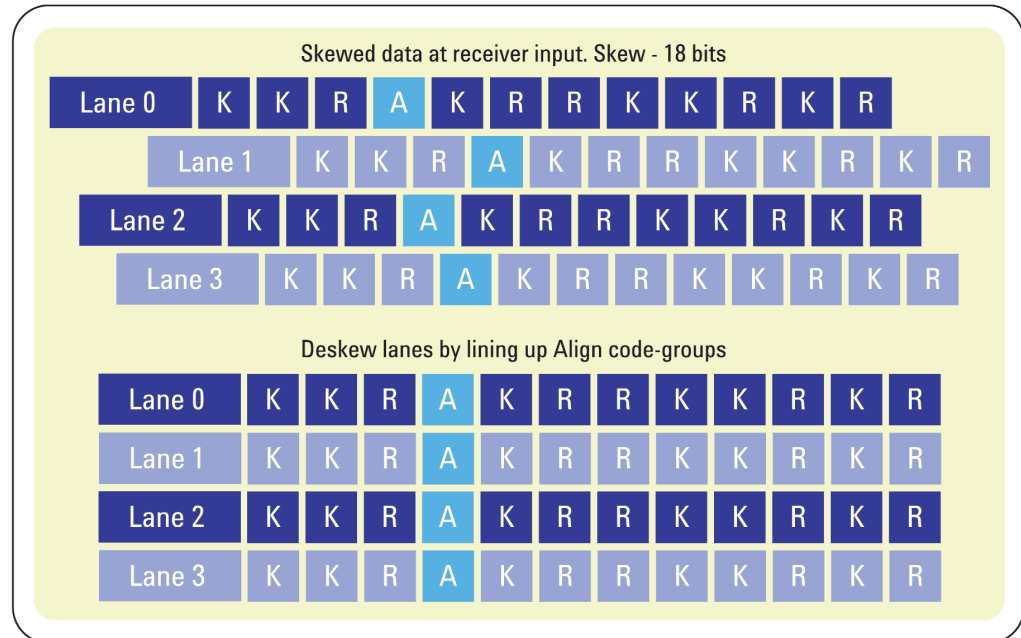


Taken from IEEE 802.3ae task force XAUI/XGXS proposal

Figure 10. Basic code groups

A separate error detector and pattern generator is required (not because the pattern generator is clocked in this application at 12.5 Gb/s and the error detector at 3.125 Gb/s – they may be clocked independently), it is because in total three different custom patterns must be used.

Before a data pattern may be supplied to the XAUI interface the four input lanes must be de-skewed or aligned. This is a two stage process – first internal synchronisation of four lanes is acquired individually and then the lanes are de-skewed by aligning up the de-skew code/pattern contained in an idle pattern. This is shown in Figure 11, where byte /A/ is the lane de-skew byte. BER measurements are required to be performed on the data pattern and not the idle/de-skew pattern. One way of arranging this is to use the 71612C ‘alternate pattern’ mode of operation; this allows the creation and generation of two different synchronously selectable patterns. For convenience these two selectable patterns will be called pattern A_p and B_p – where ‘p’ indicates the pattern actually programmed into the pattern generator editor. In Figures 8 and 9 patterns A and B are the actual patterns at the device under test XAUI input, and C the pattern produced at the XAUI output. Pattern A is the required data stream supplied to the XAUI ASIC and is used for BER measurement. However initially Pattern B is transmitted; then the standard sequence of bytes (idle/sync, de-skew and start-of-data codes) is sent through the ASIC to allow the four lanes to de-skew properly. Once the data is running continuously the 3.125 Gb/s outputs will just be 8B/10B coded data and therefore may be BER tested with a custom RAM pattern programmed into the 71612C error detector (pattern C of Figure 8). Although the idle pattern shown in Figure 11 depicts a repeating pattern of /A/K/R/ bytes, the /R/ byte which is used for clock tolerance compensation is not required because the clocks used in the test configurations shown in Figures 8 and 9 are synchronously locked together.



Taken from IEEE 802.3ae task force XAUI/XGXS proposal

Figure 11. XGXS Deskew

Three custom patterns are required to test the XAUI interface because Patterns A_p and B_p are created/programmed as 12.5 Gb/s serial patterns in such a way that the required patterns are effectively 'demuxed down' to the 3.125 Gb/s sub-rate outputs. The first bit appears on lane zero, the second bit on lane one, the third bit on lane two and the fourth bit on lane three. The fifth bit will go to lane zero and so on. If for example the required data input pattern (A) to the four XAUI lanes is a 0101010101...pattern, then this would also be the expected error free pattern produced by the XAUI output lanes. It would therefore also be the same as pattern C. Pattern C is programmed into the error detector as the reference pattern for error detection. However, it is NOT the same as pattern A_p , because in order to generate 0101010101... at each subrate output, pattern A_p is programmed in the pattern generator as 000011110000111100001111....etc. This also explains why an integrated generator and analyzer (71612C option UHF) may not be used. When 'alternate pattern' mode is selected on the 71612C option UHF the error detector ALWAYS uses pattern A_p as the reference pattern for bit-by-bit error detection. Consequently the integrated configuration - option UHF, would not allow the expected XAUI output pattern 0101010101.. to be used as the reference pattern for error detection – a separate error detector must therefore be used.

XAUI test patterns

High frequency test pattern

This pattern is intended to be used to test random jitter (RJ) at a BER of 10^{-12} and also to test the asymmetry of transition times; it is not intended for jitter compliance testing. The pattern generates an alternating one zero pattern on each XAUI input lane 01010101010101....etc. This pattern represents the continual transmission of the D21.5 code-group on each XAUI lane. The high frequency test pattern would be programmed into the 71612C pattern generator as 0000111100001111000011110000....etc.

Low frequency test pattern

This pattern consists of alternating groups of five ones and five zeros 1111100000111110000011111.... It is intended to be used to test low frequency RJ and to test phase lock loop tracking error. This pattern represents the continual transmission of the K28.7 code-group on each XAU1 lane. The low frequency test pattern would be programmed into the 71612C pattern generator as follows:

Sub-rate 0
Sub-rate 1
Etc.

The diagram illustrates a multi-rate system where each sub-rate has its own set of bits. The top row, labeled "Sub-rate 0", consists of a sequence of 1s followed by 0s. The second row, labeled "Sub-rate 1", also consists of a sequence of 1s followed by 0s. The third row, labeled "Etc.", shows a similar pattern. This visualizes how different sub-rates can coexist and share a common time slot or resource allocation.

Mixed frequency test pattern

This pattern is intended to test the combination of RJ and deterministic jitter (DJ) due to high frequency ISI; it is not intended for jitter compliance testing. The pattern is repeated continuously on each XAUI lane (or 71612C sub-rate outputs) for the duration of the test. The required sub-rate pattern is as follows:

1111101011 0000010100.
This pattern would be programmed into the 71612C as:
1111111111111111111000011110000111111100000000000000000000011110000111100000000

Continuous random test pattern (CRPAT)

This pattern is more complex and difficult to document in this paper. The un-coded version of the pattern (1512 data octets) is described in hexadecimal format in 802.3ae annex 48A. It provides broad spectral content and minimal peaking and may be used for the measurement of jitter at either a system level or component level. Again this pattern should not be used for jitter compliance testing. This (alternate) pattern is available as a down load on the 71612C web-page created so that the required coded CRPAT pattern is produced at the 71612C sub-rate outputs (or XAUI lanes).

Continuous jitter test pattern(CJPAT)

This pattern is also complex; the above comments also apply except that this pattern is intended to be used for jitter compliance testing. The un-coded version is 1528 data octets long. It is intended to stress the receiver's clock/data recovery circuit to large instantaneous phase jumps.

Alternate patterns to allow de-skew/idle pattern to precede the sending of the data pattern

It was explained above that the 'alternate pattern' mode of operation of the 71612C is used to de-skew the XAUI lanes in the ASIC before performing BER measurements on the data pattern. Pattern A_p is programmed as described above using the 71612C editor, and pattern B_p is programmed so that the required standard /A/K/ bytes (and/R/ byte if required) are produced at the 71612C sub-rate outputs. The high frequency test pattern described above will be used as an example of the required alternative pattern B_p.

High frequency test pattern as programmed as pattern A_n in 'alternate pattern' mode:

Pattern A_p 0000111100001111000011110000...
Sub-rate $0,1,2,3$ 0 1 0 1 0 1 0...

Pattern B_p 00000000111111111111111111111111000011110000111111111000000000000000
 000011110000111100000000111111111111111111...

The sub-rate outputs would output every fourth bit as follows:

0011111010 1100000101 00111110101100000101...
 -K28.5 +K28.5 -K28.5

This is the required repeating K28.5 Sync or 'K' word taking account of running disparity rules for the 8B/10B transmission code. Positive and negative running disparity is fully explained in section 11 of the Fibre Channel FC-PH document. The tables of valid data characters and valid special characters may also be found in section 11 of this document.

This K word is repeated 16 times (ending at bit 639) followed by one repetition of the align word – the A word (K28.3).

Following running disparity rules the A word (K28.3) is programmed into pattern B_p from bit 640 as:

00000000111111111111111100000000111111111111111000000000000000...
 bit 640

At the sub-rate outputs every fourth bit would be transmitted as:

0011110011 1100000101 00111110101 etc
 -K28.3 +K28.5 -K28.5 etc

The 16 × K28.5 word + 1 × K28.3 word is repeated N times; for example if N=2, then the repeated pattern ends with bit 1359. Then pattern B_p is programmed such that a valid special character is generated on lane (sub-rate) 0 as a 'start of data' character – for example –K27.7.

Pattern B_p from bit 1280:

000000001111111111111111111111110000111100001111111110000000000000001111111100000000
 111110000111100011101111000000000000111end

Sub-rate 0:

0011111010 1100001100 1101101000
 -K28.5 +K28.3 -K27.7 start of data word

Sub-rates 1,2 and 3:

0011111010 1100001100 1010110001
 -K28.5 + K28.3 the last 'word' may be any valid character (eg -D31.7)

(Note that the alternate pattern mode is also used for the generation of CRPAT and CJPAT. Because BER testing is not performed on the start/preamble/start-of-frame delimiter octets these are programmed as pattern B_p in the 71612C and the required RPAT test sequence is programmed as pattern A_p in the 71612C.)

10G optical test configuration and patterns

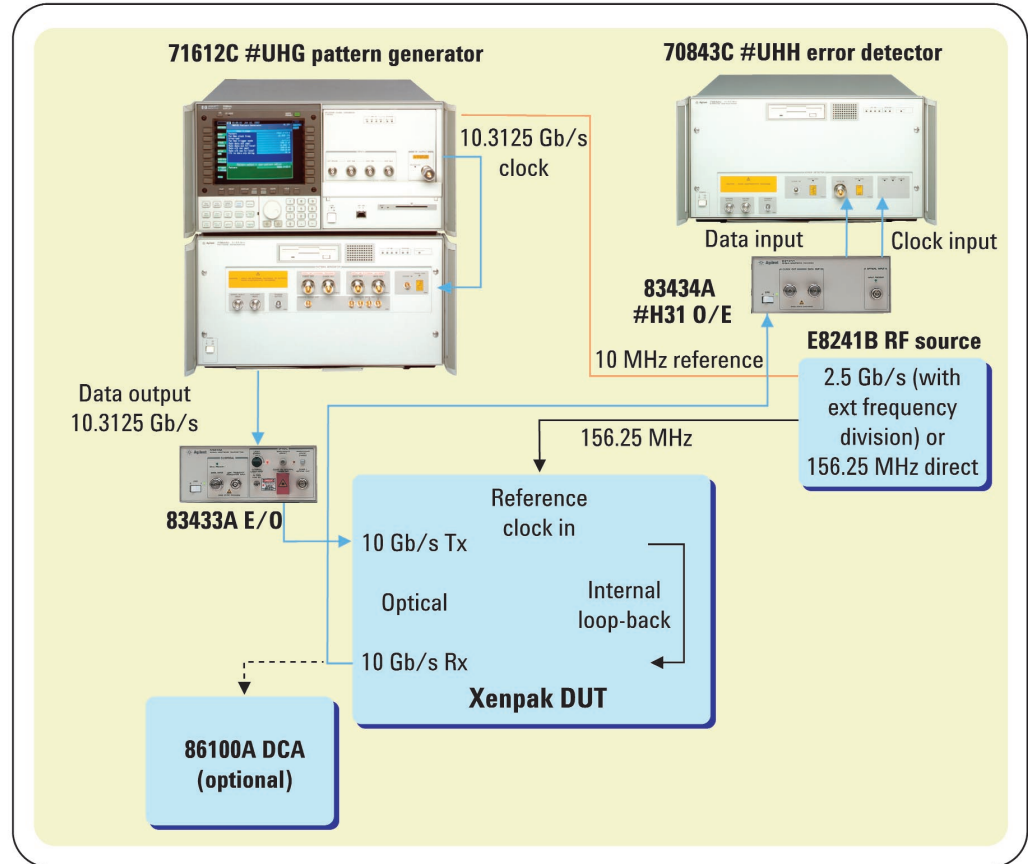


Figure 12. 10GbE device testing at 10.3125 Gb/s

Figures 12 and 13 shows the configuration used to test a Xenpak device at the 10Gb/s optical I/O. In the introduction to this paper the testing philosophy was explained and reasons stated for independent testing at the 3.125 Gb/s XAUI and 10.3125 Gb/s interfaces rather than from 3.125 Gb/s to 10.3125 Gb/s and vice versa.

For this test an internal loop-back mode is established via the MDIO management interface, and the 83433A lightwave transmitter and 83434A lightwave receiver used to convert the electrical I/O of the 71612C to optical. The operational wavelength of the 83433A lightwave source is 1552 nm; this test configuration therefore may not be used to test devices intended to operate at 850 nm and 1310 nm.

With the internal loop back mode activated any test pattern may be used, for example a $2^{31}-1$ PRBS.

Customers who are exclusively testing at 10.3125 Gb/s and do not require to test at the XAUI interface may use the 71612C option UHF (combined pattern generator and error detector) in place of the 71612C option UHG and 70843C option UHH.

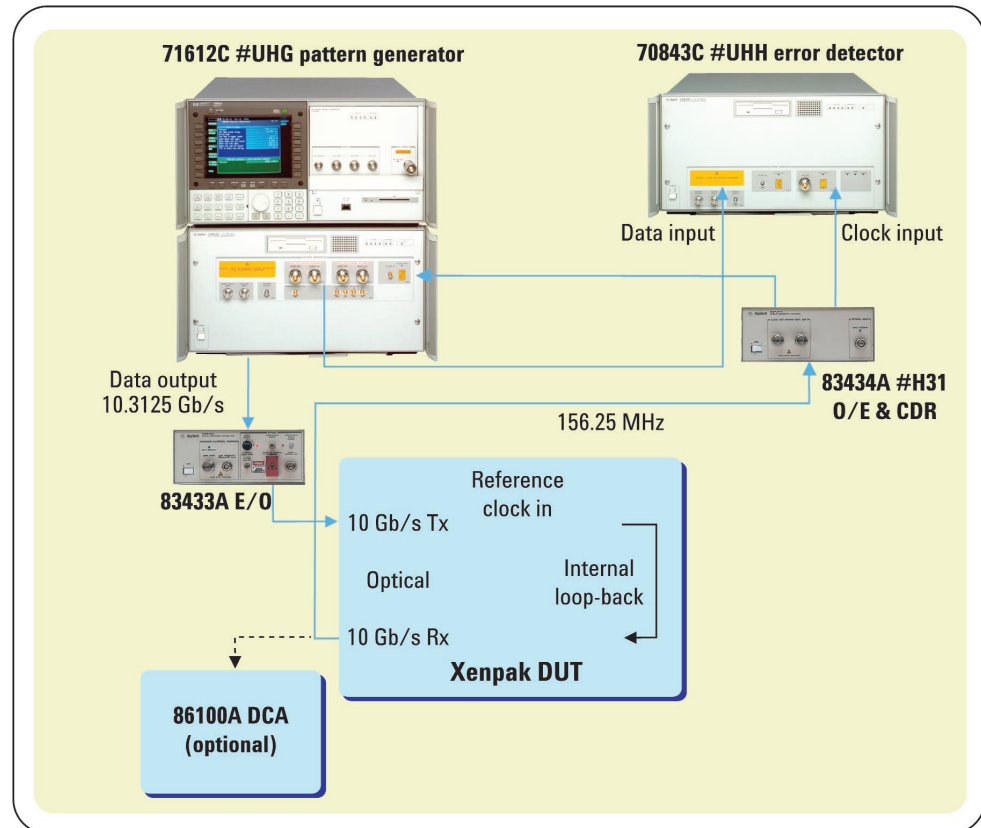


Figure 13. 10GbE device testing at 10.3125 Gb/s

Jitter testing for XAUI and 10GBASE-R and 10GBASE-W interfaces

XAUI Jitter Tolerance

IEEE 802.3ae/D5.0 requires the XAUI receiver to have a peak-peak total jitter amplitude tolerance of at least 0.65 UI. This total jitter consists of components of deterministic jitter, random jitter and additional sinusoidal jitter. Deterministic jitter tolerance should be at least 0.37 UIp-p. Deterministic and random jitter tolerance should be at least 0.55 UIp-p. In addition, the XAUI receiver should also tolerate a sinusoidal jitter component defined by the mask shown in Figure 14.

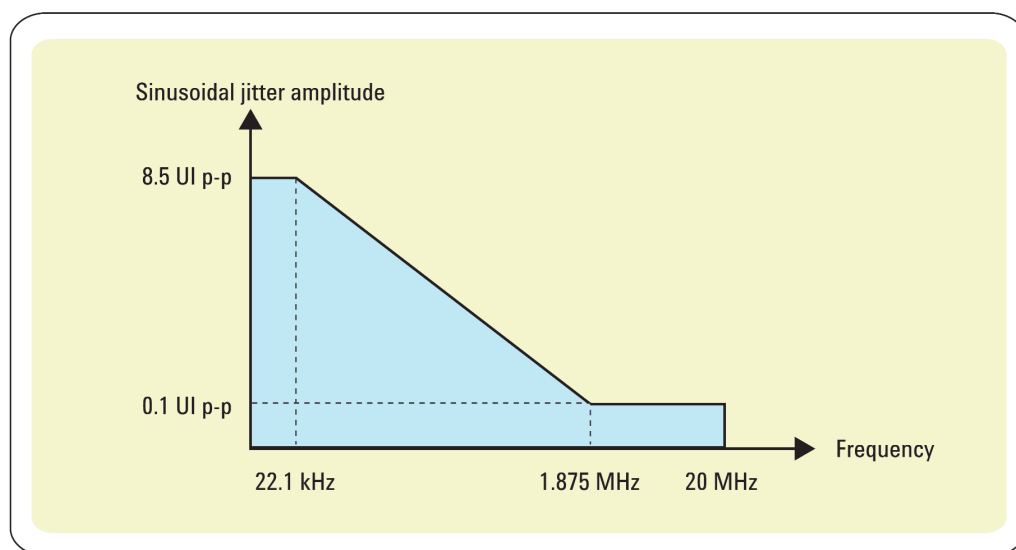


Figure 14. Single-tone sinusoidal jitter mask

Note that the combination of the 71612C and the 71501D (frequency agile) jitter analyzer, allows sinusoidal jitter complying with the template of Figure 14 to be generated by the 71612C.

The data pattern used for jitter measurements is the CJPAT discussed above, and defined in Annex 48A of 802.3ae. This pattern is available on the 71612C web page in two forms suitable for downloading to the pattern generator and the error detector.

IEEE 802.3ae requires that transmitter jitter measurement should be evaluated with a “bathtub curve”. A bit error ratio test set (BERT) such as the 71612C horizontally scans the horizontal eye opening across the eye centerline and measures the BER at each point in time. The plot of BER as a function of sampling time is known as a “bathtub curve”. This BERT scan technique can provide random and deterministic jitter components and also is an effective method of predicting low BER without impractically long test times. Further details may be found in Annex 48B of 802.3ae.

Jitter testing for 10GBASE-R and 10GBASE-W

This is discussed in detail in 802.3ae and only a synopsis will be given here. Acceptable transmitted jitter is achieved by compliance with the requirements of the 'transmitter eye mask' and 'transmitter and dispersion penalty' clauses of the draft standard. Acceptable receiver jitter tolerance is achieved by compliance with the requirements of the 'stressed receiver conformance test'. The latter includes a component of sinusoidal jitter, the template of which is being defined at this time.

Many of the 802.3ae optical measurements require the use of the Xenpak internal test pattern generator and pattern checker (error detector). The Standard requires two types of test pattern; square wave and pseudo-random. A pattern consisting of four (10GBASE-R) to eleven (10GBASE-W) consecutive ones followed by an equal run of zeros is recommended for the square wave.

The two pseudo-random test patterns for 10GBASE-R are assembled from specified segments generated dynamically using the 58 bit scrambler using defined starting seeds. The Standard defines how the segments are assembled into 33792 bit patterns which may be held in the BERT custom pattern memory or generated or detected by the Xenpak internal test pattern generator and pattern checker. One pattern represents typical scrambled data while the other represents a less typical pattern which could happen by chance and is believed to be more demanding of the transmission process including the clock recovery system. There is also an optional PRBS 31 test pattern which may be used for some transmitter and receiver tests. The polynomial for this is $G(x) = 1 + x^{28} + x^{31}$ which is compatible with the 71612C pattern generator and error detector. Examples of the use of the internal test pattern generator include (Xenpak) transmitter optical eye and transmitter jitter testing. The eye test uses either the custom 'typical scrambled data' pseudo-random test pattern or the optional PRBS31 pattern; the transmitter jitter test requires the use of the 'more demanding' pseudo-random pattern or the optional PRBS31 pattern. (These transmitter tests may also be performed using the 71612C with the Xenpak in internal loop-back mode as shown in Figures 12 and 13.) The stressed receiver jitter conformance test requires the use of the (Xenpak) receiver of the system under test; the 71612C pattern generator may be used to continuously generate the required test pattern (either the 'more demanding' pseudo random test pattern or the optional PRBS31 pattern).

In the case of 10GBASE-W, 802.3ae also requires the WIS (WAN interface sub-layer) to include a test pattern generator and pattern checker. Defined serial test patterns allow the 10GBASE-W PMA and PMD sub-layers to be tested for compliance in a system environment. In addition to the square wave test pattern and the PRBS31 pattern referred to above, a mixed frequency test pattern is also defined. The mixed frequency test pattern will not be described in detail; it is based on the Test Signal Structure of ITU-T Recommendation O. 172, 1999 with a Consecutive Identical Digit pattern defined by ITU-T Recommendation G.957, 1995. The WIS Transmit process is used to generate the mixed frequency pattern with the SPE payload filled by a $2^{23}-1$ PRBS. For increased testing flexibility these patterns may be stored in the custom pattern memory of the 71612C pattern generator and error detector.

References

Acronyms

ASIC	Application-specific integrated circuit
BER	Bit error ratio
BERT	Bit error ratio test-set
CJPAT	Continuous jitter test pattern
CRPAT	Continuous random test pattern
DJ	Deterministic jitter
DUT	Device under test
ISI	Inter-symbol interference
LAN	Local area network
MAN	Metropolitan area network
MAC	Media access control
MDI	Medium dependent interface
MDIO	Management data input/output
MSA	Multi-source agreement
PCS	Physical coding sub-layer
PLL	Phase-locked-loop
PMA	Physical medium attachment
PMD	Physical medium dependent
PRBS	Pseudo-random binary sequence
OSI	Open systems interconnection
RJ	Random jitter
SDH	Synchronous digital hierarchy
SONET	Synchronous optical network
UI	Unit interval
WAN	Wide area network
WIS	WAN interface sub-layer
WWDM	Wide wavelength division multiplex
XENPAK	10 Gigabit Ethernet MSA
XGMII	10 Gigabit media independent interface
XSBI	10 Gigabit sixteen bit interface
XAU1	10 Gigabit attachment unit interface

Useful URLs

71612C 12.5 Gb/s error performance analyzer
www.agilent.com/cm/rdmfg/hsber

10 Gigabit Ethernet Alliance
<http://www.10gea.org>

XENPAK Multi-source Agreement
<http://www.xenpak.org>

IEEE 802 LAN/MAN Standard Committee
<http://grouper.ieee.org/groups/802/index.htm>

Download IEEE 802™ Standards
<http://standards.ieee.org/getieee802/>

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<http://grouper.ieee.org/groups/802/3/index.html>

IEEE 802.3ae Task Force
<http://grouper.ieee.org/groups/802/3/ae/index.html>

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